UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,727	12/28/2001	Stefan Johannes Bitterlich	9824-0077-999	2597

38881 7590 08/22/2006	EXAMINER
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DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>09 May 2006</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-37</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-37</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   In view of the Pre-appeal Brief filed on 5/9/06, PROSECUTION IS HEREBY

REOPENED. Accordingly, a non-final Office Action is set forth below.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Subramanian et

al (2002/0015401), previously cited.

The applied reference has a common assignee with the instant application. Based upon

the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C.

102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37

CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the

inventor of this application and is thus not the invention "by another," or by an appropriate

showing under 37 CFR 1.131.

-Regarding to claim 1, Subramanian et al discloses a channel CODEC processor (104)

(see figure 1B) wherein the channel CODEC processor can be implemented with a processor

(102a) (shown in figure 2A) to operate (see [0060]), channel CODEC processor comprising:

an algorithm-specific kernel block (comprising (273a) of (K1261a) (see figure 2D))

configurable to receive a data stream (278), the kernel block comprising logic tailored to perform

at least one step of a channel CODEC algorithm on the data stream (e.g., to perform one of

"codec functions" (see [0062]), (see also [0060, 0078, 0079, 0083, 0085]); and

a processor core (comprising ((219) (see figure 2A) and ((272) (see figure 2D))

configurable to provide configuration data to the algorithm-specific kernel block, the

configuration data causing the kernel block to perform the at least one step of the channel

CODEC algorithm according to one of a plurality of wireless communication standards (e.g.,

TDMA standards) as specified by the configuration data (see [0031, 0033, 0037, 0042, 0043,

0051, 0053, 0060-0062, 0079-0080].

-Regarding to claim 2, Subramanian et al discloses an interconnect (comprising ((276)

(see figure 2D)) and ((204a) (see figure 2C)) through which data flows between the processor

core and the algorithm-specific kernel block, wherein the processor core is operable to provide

configuration data to the interconnect to control data-flow between the processor core and the

algorithm-specific kernel block (see [0075-0077, 0079]).

-Regarding to claim 3, Subramanian et al discloses that the configuration data controls

operation parameters of the algorithm-specific kernel block (see [0102]).

-Regarding to claim 4, Subramanian et al discloses that the processor core is operable to

perform time-multiplexed operations for a plurality of concurrent channel CODEC tasks (see

[0033, 0043, 0082, 0158, , 0174, 0188]).

-Regarding to claim 5, Subramanian et al discloses that the processor core is operable to

perform another step of the channel CODEC algorithm (e.g, to perform steps of one of "codec

functions" (see [0062]).

-Regarding to claim 6, Subramanian et al discloses that the processor core is operable to perform steps of another channel CODEC algorithm (e.g, to perform steps of another one of "codec functions" (see [0062]).

-Regarding to claim 7, Subramanian et al discloses a local memory (272, 271) (see figure 2D) coupled to the processor core (see [0080, 0084]).

-Regarding to claim 8, Subramanian et al discloses a local memory (272, 271) coupled to the algorithm-specific kernel block (see [0080, 0084]).

-Regarding to claim 9, Subramanian et al discloses that the logic of the algorithm-specific kernel block can be tailored to decode data in the data stream according to a Viterbi decoding algorithm (418) (see figure 4, [0153, 0155]).

-Regarding to claim 10, Subramanian et al discloses that the logic of the algorithm-specific kernel block can be tailored to decode data in the data stream according to a convolutional decoding algorithm (418) (see figure 4, [0153, 0155]).

-Regarding to claim 11, Subramanian et al discloses that the logic of the algorithm-specific kernel block can be tailored to decode data in the data stream according to a Turbo decoding algorithm (420) (see figure 4).

-Regarding to claim 12, Subramanian et al discloses that the algorithm-specific kernel block comprises a reconfigurable encoder "convolution encoder" for convolutional codes in which at least one polynomial parameter of the encoder is controlled by the configuration data (see [0158]).

-Regarding to claim 13, Subramanian et al discloses that the algorithm-specific kernel block comprises a reconfigurable encoder "Turbo encoder" for Turbo codes in which at least one polynomial parameter of the encoder is controlled by the configuration data (see [0158]).

-Regarding to claim 14, Subramanian et al discloses that the algorithm-specific kernel block can be implemented to comprise a reconfigurable cyclic-redundancy check (CRC) encoder (see (422, 406) of figure 4, [0158]).

-Regarding to claim 15, Subramanian et al discloses that wherein the algorithm-specific kernel block comprises a reconfigurable cyclic-redundancy check (CRC) checker (422) (see figure 4).

-Regarding to claim 16, as similarly applied to claims 1-14 set forth above and hereafter incorporated by reference, Subramanian et al discloses a channel CODEC processor, wherein the channel CODEC processor can be implemented with a processor (102a) (shown in figure 2A) to operate (see [0060]), the channel CODEC processor comprising:

a first algorithm-specific kernel block (comprising (270) of (K1261a) (see figure 2D)) operable to receive a data stream (278) (see figure 2D), the first algorithm-specific kernel block comprising logic tailored to perform a step (e.g., step (414) (see figure 4)) of a first channel CODEC algorithm on the data stream to generate a first processed data stream (278);

a second algorithm-specific kernel block (e.g., comprising (270) of (K2262a) (see figures 2C and 2D)) coupled to the first algorithm-specific kernel block to receive the first processed data stream, the second algorithm-specific kernel block comprising logic tailored to perform a step (e.g., step (418) (see figure 4)) of a second channel CODEC algorithm on the first processed data stream to generate a second processed data stream; and

a processor core (comprising ((219) (see figure 2A)), ((272) of (K1261A), (272) of

K2262A) (see figures 2C and 2D))) coupled to provide configuration data to the algorithm-

specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to

perform the step of the first channel CODEC algorithm and the step of the second channel

CODEC algorithm according to one of a plurality of wireless communication standards as

specified by the configuration data.

-Regarding to claim 17, Subramanian et al discloses an interconnect (comprising (204a,

276) (see figures 2C and 2D)) through which data flows among the processor core and the

algorithm-specific kernel blocks, wherein the processor core is operable to provide configuration

data to the interconnect to control data-flow among the processor core and the algorithm-specific

kernel blocks.

-Regarding to claim 18, Subramanian et al discloses that the first configuration data

controls operation parameters of the first algorithm-specific kernel block and wherein the second

configuration data controls operation parameters of the second algorithm-specific kernel block

(see figures 2D-F and 4).

-Regarding to claim 19, Subramanian et al discloses that the processor core is operable to

perform time-multiplexed operations for a plurality of concurrent channel CODEC tasks (see

[0033, 0043, 0082, 0158, 0174, 0188]).

-Regarding to claim 20, Subramanian et al discloses that the processor core is operable to

perform steps of the first channel CODEC algorithm and the second channel CODEC algorithm

(see figures 2D-F and 4).

-Regarding to claim 21, Subramanian et al discloses that the processor core is operable to perform steps of a third channel CODEC algorithm (e.g., to perform steps of a third channel CODEC algorithm (422)) (see figure 4).

-Regarding to claim 22, as similarly applied to claims 1-14 set forth above and hereafter incorporated by reference, Subramanian et al discloses a channel CODEC processor, wherein the channel CODEC processor can be implemented with a processor (102a) (shown in figure 2A) to operate (see [0060]), the channel CODEC processor comprising:

an input (input of (219) (see figure 2A)) operable to receive a data stream from (112);

a plurality of processor cores (219, 272, K1261a, K2262a) (see figures 2A, 2C, 2D) including a first processor core (219, (272) of (K1261a)) and a second processor core (219, (272) of (K2262a)) operable to process data in the data stream;

a plurality of algorithm-specific kernel blocks (e.g., ((270) of (K1261a), (270) of (K2262A)) (see figures 2C and 2D)) including a first algorithm-specific kernel block ((270) of (K1261a) and a second algorithm-specific kernel block (270) of (K2262A) coupled to the first processor core and the second processor core, respectively, wherein the first algorithm-specific kernel block is operable to receive first data from the first processor core and to perform at least one step of a first channel CODEC algorithm on the first data (278) (see figure 2D), wherein the second algorithm-specific kernel block is operable to receive second data from the second processor core and to perform at least one step of a second channel CODEC algorithm on the second data (278) (see figure 2D).

-Regarding to claim 23, Subramanian et al discloses that operation parameters of the first algorithm-specific kernel block and the second algorithm-specific kernel block are user-configurable (see [0032, 0053, 0071, 0074, 0085, 0102, 0176]).

-Regarding to claim 24, Subramanian et al discloses that at least (219) (see figure 2A) as one of the processor cores is coupled to provide configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel CODEC algorithm (e.g., (414) (see figure 4) and the step of the second channel CODEC algorithm (e.g., (418) (see figure 4) according to one of a plurality of wireless communication standards as specified by the configuration data.

-Regarding to claim 25, Subramanian et al discloses an interconnect (comprising ((276) (see figure 2D)) and ((204a) (see figure 2C)) through which data flows among the processor cores and the algorithm-specific kernel blocks, wherein at least one of the processor cores is operable to provide configuration data to the interconnect to control data-flow between the processor cores and the algorithm-specific kernel blocks.

-Regarding to claim 26, Subramanian et al discloses that the processor cores are operable to perform time-multiplexed operations for a plurality of concurrent channel CODEC tasks (see [0033, 0043, 0082, 0158, , 0174, 0188]).

-Regarding to claim 27, Subramanian et al discloses memories (272, 271) (see figure 2C) coupled to the processor cores (see [0080, 0084]).

-Regarding to claim 28, Subramanian et al discloses memories (272, 271) (see figure 2C) coupled to the algorithm-specific kernel blocks (see [0080, 0084]).

-Regarding to claim 29, as similarly applied to claims 1-14 set forth above and hereafter

incorporated by reference, Subramanian et al discloses a communication device (see figure 1B),

comprising:

an I/O interface (116) (see figure 1B) operable to couple to an antenna (120);

a modem device (102a) (see figure 1B) for modulating and demodulating data coupled to

the I/O interface; and

a channel CODEC processor (104) (see figure 1B) coupled to the modem device to

receive a demodulated data stream, wherein the channel CODEC processor can be implemented

with a processor (102a) (shown in figure 2A) to operate (see [0060]), the channel CODEC

processor comprising:

a first algorithm-specific kernel block ((270) of (K1261a) (see figure 2D)

operable to receive the demodulated data stream (278), the kernel block comprising logic

tailored to perform at least one step (418) of a channel decoding algorithm (e.g., (418,

416, 420, 422) (see figure 4)) on the demodulated data stream; and

a first processor core (219, 272) (see figures 2A and 2D) coupled to provide first

configuration data to the algorithm-specific kernel block, the configuration data causing

the kernel block to perform the at least one step of the channel decoding algorithm

according to one of a plurality of wireless communication standards as specified by the

first configuration data.

-Regarding to claim 30, Subramanian et al discloses that the first processor core is

operable to perform steps (414, 420, 422) of the channel decoding algorithm (see figure 4).

-Regarding to claim 31, Subramanian et al discloses a network interface (116, 120) (see

figure 1B) operable to receive a data stream from a network (inherently included for transmitting

the data stream to the antenna (120) for the reception of the network interface (116, 120), and

wherein the channel CODEC processor further comprises: a second algorithm-specific kernel

block (e.g., (270) of (K2262a) (see figures 2C and 2D)) operable to receive the data stream, the

kernel block comprising logic tailored to perform at least one step of a channel encoding

algorithm "convolution encoder function" corresponding to a decoding algorithm (418) (see

figure 4, {0158]) on the data stream; a second processor core (comprising (219), (270) of

(K2262a) (see figures 2A, 2C and 2D)) coupled to provide second configuration data to the

algorithm-specific kernel block, the configuration data causing the kernel block to perform the at

least one step of the channel encoding algorithm according to one of a plurality of wireless

communication standards as specified by the second configuration data.

-Regarding to claim 32, Subramanian et al discloses that the second processor core is

operable to perform steps (414, 420, 422) of the channel decoding algorithm (416, 418, 420, 422)

(see figures 4).

-Regarding to claim 33, as similarly applied to claims 1-14 and 29-32, set forth above and

hereafter incorporated by reference, Subramanian et al discloses a communication device (see

figure 1B), comprising:

an I/O interface (116) (see figure 1B) operable to couple to an antenna (120);

a modem device (102a) for modulating and demodulating data coupled to the I/O

interface; and

a channel CODEC processor (104) coupled to the modem device to receive a demodulated data stream, wherein the channel CODEC processor can be implemented with a processor (102a) (shown in figure 2A) to operate (see [0060]), the channel CODEC processor comprising:

a first algorithm-specific kernel block (comprising (270) of (K1261a) (see figure 2D)) operable to receive the demodulated data stream, the first algorithm-specific kernel block comprising logic tailored to perform a step of a first channel decoding algorithm (418) (see figure 4) on the demodulated data stream to generate a first processed data stream;

a second algorithm-specific kernel block (e.g., comprising (270) of (K2262a) (see figures 1C and 2D) coupled to the first algorithm-specific kernel block to receive the first processed data stream, the second algorithm-specific kernel block comprising logic tailored to perform a step of a second channel decoding algorithm (422) on the first processed data stream to generate a second processed data stream; and

a first processor core (comprising (219), (272) of (K1261a), (272) of (K2262a)) (see figures 2A and 2D)) coupled to provide first configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel decoding algorithm and the step of the second channel decoding algorithm according to one of a plurality of wireless communication standards as specified by the first configuration data.

-Regarding to claim 34, Subramanian et al discloses that the first processor core is operable to perform steps of the channel decoding algorithms (418, 422) (see figure 4).

-Regarding to claim 35, Subramanian et al discloses a network interface operable to receive a data stream from a network (inherently included for transmitting the data stream to the antenna (120) for the reception of the network interface) (see figure 1B).

-Regarding to claim 36, Subramanian et al discloses:

a third algorithm-specific kernel block (e.g., (270) of (K3263a), (see figures 2C and 2D)) operable to receive the data stream from the network interface, the third algorithm-specific kernel block comprising logic tailored to perform a step of a first channel encoding algorithm (e.g., "Convolution Encoder function" (see [0158]) corresponding to a decoding algorithm (418) (see figure 4) on the data stream to generate a third processed data stream;

a fourth algorithm-specific kernel block (e.g., (270) of (K4264a), (see figures 2C and 2D)) coupled to the third algorithm-specific kernel block to receive the third processed data stream, the fourth algorithm-specific kernel block comprising logic tailored to perform a step of a second channel encoding algorithm (interleave) corresponding to a decoding algorithm (414) (see figure 4, [0158]) on the first processed data stream to generate a fourth processed data stream; and

a first processor core (comprising (219), (272) of (K3263a), (272) of (K4264a)) (see figures 2A and 2D)) coupled to provide second configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel encoding algorithm and the step of the second channel encoding algorithm according to one of a plurality of wireless communication standards as specified by the second configuration data.

-Regarding to claim 37, Subramanian et al discloses that the second processor core is operable to perform steps of the channel encoding algorithms "Convolution Encoder function" and "interleave" (see [0158]).

Response to Arguments

4.   Applicant's arguments filed on 5/9/06 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (8:00 AM - 4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phuong Phu

Primary Examiner
Art Unit 2611

Phuong Phu

**PHUONG PHU
PRIMARY EXAMINER**

Phuong Phu
08/14/06